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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/945,553 | 08/30/2001 | Fernando Gonzalez | 303.775US1 | 1842 |

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| EXAMINER | |
|---|---|
| FOURSON III, GEORGE R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/945,553 | GONZALEZ ET AL. | |
| | Examiner | Art Unit | |
| | George Fourson | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *2-4,13,16,23-30 and 34-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,9-12,14,15,17-22 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/2/05 has been entered.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 31 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for thermal processing in the presence of a composition as described on instant page 16, lines 1-10, does not reasonably provide enablement for recitation of "under conditions that reduce redeposition of the metal film broadly. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to practice the invention commensurate in scope with these claims. There is no discussion of other methods of reducing redeposition and therefor insufficient guidance to enable one of ordinary skill in the art to practice the invention without undue experimentation.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Pan et al, of record.

Pan et al discloses gate reoxidation using nitride spacers to prevent metal oxidation thus reducing redeposition as recited (abstract).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan et al as applied to claim 1 above, and further in view of Jain et al.

Pan et al does not disclose presence of $NF_3$ during gate patterning.

Jain et al discloses patterning of layers to form a polycide gate electrode using $NF_3$ gas (col.2, lines 13-22).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Pan et al and Jain et al to enable the step of patterning the gate stack of Pan et al to be performed and furthermore to enable removal of the ARC as disclosed by Jain (see abstract).

Claims 1,5,6,9-12,14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art (AAPA), Mitani et al and Pan et al, of record.

Applicant admits in the instant specification, pages 1-3, formation of a polycide gate stack followed by patterning and oxidation of the polysilicon portion of the stack. The process of AAPA does not include presence of gaseous $NF_3$.

Mitani et al discloses oxidation of polysilicon gate material in an ambient comprising $NF_3$ as a method of introducing F into the channel region of a MOSFET at 600°C (col.41, lines 12-18).

Mitani et al discloses one aim of the process is introduction of the halogen element contained in the sidewall insulating films formed on the sidewalls of the gate electrode into the gate electrode (col.3, lines 65+) to obtain a desired doping profile in the channel region including a profile in which the F concentration near the edges of the channel region is higher than that in the middle of the channel region (col.42, lines 4+). Also see the 26th embodiment (col.41) in which an insulating film is formed on the sidewall of a polysilicon gate electrode by thermal oxidation of polysilicon in the presence of $NF_3$ to introduce F into the channel region of a FET. The reference also discloses that a gate stack including a sandwiched polysilicon layer can be employed in the invention (col.5, lines 19-25).

Pan et al discloses that oxidation of metal and barrier layers can be prevented in gate reoxidation when using oxidation temperatures up to 650°C (col.5, lines 1 and 2).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of AAPA and Mitani et al to enable the oxidation step of AAPA to be performed and further to achieve the introduction of F according to the teachings of Mitani et al to achieve a desired profile of F in the channel region of the resulting MOSFET. The presence of the metal restricting oxidation of the top surface of the poly region would be understood by one of ordinary skill in the art to result in the profile in which the F concentration is higher at the edges than in the middle of the channel region. One of ordinary skill in the art would have a reasonable expectation of success that the process of the combination of references relied

on in view of the teachings of Mitani that the F introduction method can be applied to a gate stack including a sandwiched polysilicon layer and in view of the teachings of Pan that a gate metal layer will not oxidize at 600°C.

Claims 17 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Mitani et al and Pan et al as applied to claims 1,5,6,9-12,14 and 15 above, and further in view of Cunningham.

AAPA in combination with Mitani et al does not include sidewall formation or metal nitride barrier layer formation.

Cunningham discloses sidewall formation after polysilicon oxidation and metal nitride barrier layer formation in a polycide gate formation process (abstract and [0030]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of AAPA, Mitani et al and Cunningham to enable the polycide gate structure of AAPA to be formed according to the teachings of Cunningham related to obtaining greater tolerance to higher temperature annealing.

Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Mitani et al and Pan et al as applied to claims 1,5,6,9-12,14 and 15 above, and further in view of Jain et al.

AAPA and Mitani et al do not disclose presence of $NF_3$ during gate patterning.

Jain et al discloses patterning of layers to form a polycide gate electrode using $NF_3$ gas (col.2, lines 13-22).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of AAPA, Mitani et al and Jain et al to enable the step of patterning the gate stack of AAPA to be performed and furthermore to enable removal of the ARC as disclosed by Jain (see abstract).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956 until 2/4/04. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner George Fourson whose telephone number is (571)272-1860. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571)272-1855. The fax number for this group is (571)273-0224 and the customer service number for group 2800 is 571-272-2800. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

George Fourson
Primary Examiner
Art Unit 2823

GFourson
July 9, 2005